What is claimed is:

1. An electronic packaging assembly, comprising:

a silicon interposer having first and second sides;

at least one semiconductor chip on a first side of the silicon interposer, wherein the semiconductor chip on the first side of the silicon interposer is further coupled to a Peltier element;

at least one semiconductor chip on a second side of the silicon interposer; and

a number of electrical connections through the silicon interposer wherein the number of electrical connections couple the semiconductor chips located on each side of the silicon interposer.

2. The electronic packaging assembly of claim 1, wherein the at least one semiconductor chip on the first side of the silicon interposer includes a microprocessor chip.

3. The electronic packaging assembly of claim 1, wherein the Peltier element includes a Copper (Cu) to a p-type semiconductor junction.

4. The electronic packaging assembly of claim 3, wherein the p-type semiconductor is selected from the group consisting of p-doped Bismuth Telluride (Bi_3Te_2), p-doped Lead Telluride (PbTe), and p-doped Silicon Germanium (SiGe).

5. The electronic packaging assembly of claim 1, wherein the Peltier element includes a Copper (Cu) to an n-type semiconductor junction.

6. The electronic packaging assembly of claim 5, wherein the n-type semiconductor is selected from the group consisting of n-doped Bismuth Telluride (Bi_3Te_2), n-doped Lead Telluride (PbTe), and n-doped Silicon Germanium (SiGe).

7. The electronic packaging assembly of claim 1, wherein the at least one semiconductor chip on the second side of the silicon interposer includes a memory chip.

8. The electronic packaging assembly of claim 7, wherein the memory chip is an electronically erasable and programmable read only memory (EEPROM) chip.

9. An electronic system module, comprising:

a silicon interposer having opposing surfaces;

a microprocessor, having a circuit side, the circuit side facing a first one of the opposing surfaces of the silicon interposer, and wherein the microprocessor on the first side of the silicon interposer is further coupled to a metal-to-semiconductor junction;

a memory chip, having a circuit side, the circuit side facing a second one of the opposing surfaces of the silicon interposer; and

a number of electrical connections extending through the silicon interposer, the number of electrical connections coupling the circuit side of the microprocessor to the circuit side of the memory chip.

10. The electronic system module of claim 9, wherein the semiconductor includes an n-doped complex oxide.

11. The electronic system module of claim 10, wherein the n-doped complex oxide includes Strontium (Sr).

12. The electronic system module of claim 10, wherein the n-doped complex oxide includes Titanium (Ti).

13. The electronic system module of claim 10, wherein the n-doped complex oxide possesses an oxygen deficiency.

14. The electronic system module of claim 9, wherein the semiconductor includes a p-doped complex oxide.

15. The electronic system module of claim 9, wherein the semiconductor has at least a 0.6 coefficient of performance (COP).

16. The electronic system module of claim 9, wherein the semiconductor includes an n-doped superlattice comprising alternating layers of $(PbTeSe)_m$ and $(BiSb)_n$ where m and n are the number of PbTeSe and BiSb monolayers per superlattice period.

17. The electronic system module of claim 9, wherein the semiconductor includes a semiconductor alloy formed between Antimony (Sb) and a transition metal (T) from Group VIII, including Cobalt, Rhodium, and Iridium (Co, Rh, and Ir), and wherein the alloy has the general formula TSb_3.

18. The electronic system module of claim 17, wherein the semiconductor alloy includes a skutterudite-type crystal lattice.

19. An electronic packaging assembly, comprising:

a silicon interposer having first and second sides;

at least one semiconductor chip on a first side of the silicon interposer, wherein the semiconductor chip on the first side of the silicon interposer is further coupled to a metal-to-semiconductor junction, wherein the semiconductor is selected from the group consisting of n or p-doped Bismuth Telluride (Bi_3Te_2), n or p-doped Lead Telluride (PbTe), and n or p-doped Silicon Germanium (SiGe);

at least one semiconductor chip on a second side of the silicon interposer; and

a number of electrical connections through the silicon interposer wherein the number of electrical connections couple the semiconductor chips located on each side of the silicon interposer.

20. The electronic system module of claim 19, wherein the at least one semiconductor chip on the first side of the silicon interposer includes a microprocessor chip.

21. The electronic system module of claim 19, wherein the at least one semiconductor chip on the second side of the silicon interposer includes a memory chip.

22. The electronic system module of claim 19, wherein the semiconductor has at least a 0.6 coefficient of performance (COP).

23. An electronic system module, comprising:

a silicon interposer having opposing surfaces;

a microprocessor, having a circuit side, the circuit side facing a first one of the opposing surfaces of the silicon interposer, and wherein the microprocessor on the first side of the silicon interposer is further coupled to a metal-to-semiconductor junction, wherein the semiconductor includes either an n or p-doped complex oxide;

a memory chip, having a circuit side, the circuit side facing a second one of the opposing surfaces of the silicon interposer; and

a number of electrical connections extending through the silicon interposer, the number of electrical connections coupling the circuit side of the microprocessor to the circuit side of the memory chip.

24. The electronic system module of claim 23, wherein the doped complex oxide includes Strontium (Sr).

25. The electronic system module of claim 23, wherein the doped complex oxide includes Titanium (Ti).

26. The electronic system module of claim 23, wherein the doped complex oxide possesses an oxygen deficiency.

27. An electronic system module, comprising:

a silicon interposer having opposing surfaces;

a microprocessor, having a circuit side, the circuit side facing a first one of the opposing surfaces of the silicon interposer, and wherein the microprocessor on

the first side of the silicon interposer is further coupled to a Peltier element, wherein the Peltier element includes either an n or p-doped superlattice comprising alternating layers of $(PbTeSe)_m$ and $(BiSb)_n$ where m and n are the number of PbTeSe and BiSb monolayers per superlattice period;

a memory chip, having a circuit side, the circuit side facing a second one of the opposing surfaces of the silicon interposer; and

a number of electrical connections extending through the silicon interposer, the number of electrical connections coupling the circuit side of the microprocessor to the circuit side of the memory chip.

28. The electronic system module of claim 27, wherein the Peltier element has at least a 0.6 coefficient of performance (COP).

29. An electronic system module, comprising:

a silicon interposer having first and second sides;

at least one semiconductor chip on a first side of the silicon interposer, wherein the semiconductor chip on the first side of the silicon interposer is further coupled to a metal-to-semiconductor junction, wherein the semiconductor includes either an n or p-doped semiconductor alloy formed between Antimony (Sb) and a transition metal (T) from Group VIII, including Cobalt, Rhodium, and Iridium (Co, Rh, and Ir), and wherein the alloy has the general formula TSb_3;

at least one semiconductor chip on a second side of the silicon interposer; and

a number of electrical connections through the silicon interposer wherein the number of electrical connections couple the semiconductor chips located on each side of the silicon interposer.

30. The electronic system module of claim 29, wherein the semiconductor alloy includes a skutterudite-type crystal lattice;

31. The electronic system module of claim 29, wherein the semiconductor alloy has at least a 0.6 coefficient of performance (COP).

32. The electronic system module of claim 29, wherein the at least one semiconductor chip on the first side of the silicon interposer includes a microprocessor chip.

33. The electronic system module of claim 29, wherein the at least one semiconductor chip on the second side of the silicon interposer includes a memory chip.

34. An electronic packaging assembly, comprising:

a silicon interposer having first and second sides;

at least one semiconductor chip on a first side of the silicon interposer, wherein the semiconductor chip on the first side of the silicon interposer is further coupled to a metal-to-semiconductor junction, and wherein the metal-to-semiconductor junction coupled to the at least one semiconductor chip on the first side of the silicon interposer draws thermal energy to the semiconductor chip when a current is passed through the junction;

at least one semiconductor chip on a second side of the silicon interposer; and

a number of electrical connections through the silicon interposer wherein the number of electrical connections couple the semiconductor chips located on each side of the silicon interposer.

35. An electronic packaging assembly, comprising:

a silicon interposer having first and second sides;

at least one semiconductor chip on a first side of the silicon interposer, wherein the semiconductor chip on the first side of the silicon interposer is further coupled to a metal-to-semiconductor junction, and wherein the metal-to-semiconductor junction coupled to the at least one semiconductor chip on the first side of the silicon interposer draws thermal energy away from the semiconductor chip when a current is passed through the junction;

at least one semiconductor chip on a second side of the silicon interposer; and

a number of electrical connections through the silicon interposer wherein the number of electrical connections couple the semiconductor chips located on each side of the silicon interposer.

36. The electronic packaging assembly of claim 35, wherein the at least one semiconductor chip on the first side of the silicon interposer includes a microprocessor chip.

37. The electronic packaging assembly of claim 35, wherein the metal-to-semiconductor junction includes a Copper (Cu) to a p-type semiconductor junction.

38. The electronic packaging assembly of claim 37, wherein the p-type semiconductor is selected from the group consisting of p-doped Bismuth Telluride (Bi_2Te_3), p-doped Lead Telluride (PbTe), and p-doped Silicon Germanium (SiGe).

39. The electronic packaging assembly of claim 35, wherein the metal-to-semiconductor junction includes a Copper (Cu) to an n-type semiconductor junction.

40. The electronic packaging assembly of claim 39, wherein the n-type semiconductor is selected from the group consisting of n-doped Bismuth Telluride (Bi_2Te_3), n-doped Lead Telluride (PbTe), and n-doped Silicon Germanium (SiGe).

41. An electronic system, comprising:

an electronic packaging assembly, the electronic packaging assembly including:

a silicon interposer having first and second sides;

at least one semiconductor chip on a first side of the silicon interposer, wherein the semiconductor chip on the first side of the silicon interposer is further coupled to a Peltier element;

at least one semiconductor chip on a second side of the silicon interposer; and

a number of electrical connections through the interposer wherein the number of connections couple the semiconductor chips located on each side of the silicon interposer;

a number of external devices; and

a system bus, wherein the system bus couples the electronic packaging assembly to the number of external devices.

42. The electronic system of claim 41, wherein the at least one semiconductor chip on the first side of the silicon interposer includes a microprocessor chip.

43. The electronic system of claim 41, wherein the at least one semiconductor chip on the second side of the silicon interposer includes a memory chip.

44. The electronic system of claim 41, wherein the number of electrical connections includes a number of micro-machined vias.

45. The electronic system of claim 41, wherein the Peltier element is selected from the group consisting of doped Bismuth Telluride (Bi_2Te_3), doped Lead Telluride (PbTe), includes doped Silicon Germanium (SiGe), and a doped complex oxide.

46. The electronic system of claim 41, wherein the Peltier element has at least a 0.6 coefficient of performance (COP).

47. A method for forming an electronic packaging assembly, comprising:

forming a silicon interposer, wherein the interposer includes micro-machined vias formed through the silicon interposer;

attaching a number of flip chips to the silicon interposer, wherein the flip chips couple to the micro-machined vias; and

coupling a Peltier element to at least one of the flip chips.

48. The method of claim 47, wherein attaching a number of flip chips to the silicon interposer includes:

coupling a microprocessor chip to the silicon interposer; and

coupling a memory chip to the silicon interposer.

49. The method of claim 48, wherein coupling a memory chip to the silicon interposer includes coupling a dynamic random access memory (DRAM) chip to the silicon interposer.

50. The method of claim 48, wherein the method further includes coupling capacitor to the silicon interposer.

51. The method of claim 47, wherein coupling a Peltier element to at least one of the flip chips includes coupling a Copper (Cu) and p-type semiconductor junction to the flip chip.

52. The method of claim 51, wherein coupling a Copper (Cu) and p-type semiconductor junction to the flip chip includes coupling a p-type semiconductor selected from the group consisting of p-doped Bismuth Telluride (Bi_2Te_3), p-doped Lead Telluride (PbTe), and p-doped Silicon Germanium (SiGe).

53. The method of claim 47, wherein coupling a Peltier element to at least one of the flip chips includes coupling a Copper (Cu) and n-type semiconductor junction to the flip chip.

54. The method of claim 53, wherein coupling a Copper (Cu) and n-type semiconductor junction to the flip chip includes coupling an n-type semiconductor selected from the group consisting of n-doped Bismuth Telluride (Bi_3Te_2), n-doped Lead Telluride (PbTe), and n-doped Silicon Germanium (SiGe).

55. A method for packaging an integrated circuit, comprising:

providing a silicon interposer having opposing sides;

coupling a semiconductor chip to each of the opposing sides of the silicon interposer;

coupling the semiconductor chips on each side of the silicon interposer to one another through the silicon interposer by a number of micro-machined vias, wherein the micro-machined vias provide electrical connections between the opposing sides of the silicon interposer; and

coupling a Peltier element to at least one of the of the semiconductor chips.

56. The method of claim 55, wherein coupling the Peltier element to at least one of the semiconductor chips includes coupling a metal-to-semiconductor Peltier element, wherein the semiconductor includes either an n or p-doped semiconductor alloy formed between Antimony (Sb) and a transition metal (T) from Group VIII, including Cobalt, Rhodium, and Iridium (Co, Rh, and Ir), and wherein the alloy has the general formula Tsb_3.

57. The method of claim 55, wherein coupling the Peltier element to at least one of the semiconductor chips includes coupling a metal-to-semiconductor Peltier element, wherein the semiconductor includes either an n or p-doped superlattice comprising alternating layers of $(PbTeSe)_m$ and $(BiSb)_n$ where m and n are the number of PbTeSe and BiSb monolayers per superlattice period.

58. The method of claim 55, wherein coupling the Peltier element to at least one of the semiconductor chips includes coupling a metal-to-semiconductor Peltier element, wherein the semiconductor is a doped complex oxide.

59. The method of claim 55, wherein coupling the Peltier element to at least one of the semiconductor chips includes coupling a metal-to-semiconductor Peltier element, wherein the semiconductor is selected from the group consisting of n-doped Bismuth Telluride (Bi_2Te_3), n-doped Lead Telluride (PbTe), and n-doped Silicon Germanium (SiGe).

60. The method of claim 55, wherein coupling a semiconductor chip to each of the opposing sides of the silicon interposer includes attaching a microprocessor chip to the first side of the silicon interposer.

61. The method of claim 55, wherein coupling a semiconductor chip to each of the opposing sides of the silicon interposer includes attaching a DRAM chip to a second side of the silicon interposer.

62. A method for packaging an integrated circuit, comprising:

providing a silicon interposer having opposing sides;

coupling a semiconductor chip to each of the opposing sides of the silicon interposer;

coupling the semiconductor chips on each side of the silicon interposer to one another through the silicon interposer by a number of micro-machined vias, wherein the micro-machined vias provide electrical connections between the opposing sides of the silicon interposer;

coupling a metal-to-semiconductor junction to at least one of the of the semiconductor chips, wherein the semiconductor includes a doped complex oxide semiconductor.

63. The method of claim 62, wherein coupling a doped complex oxide semiconductor includes coupling an n-doped complex oxide semiconductor comprising Strontium (Sr) and Titanium (Ti).

64. The method of claim 62, wherein coupling a doped complex oxide semiconductor includes coupling an oxygen deficient n-doped complex oxide semiconductor.

65. A method for packaging an integrated circuit, comprising:

providing a silicon interposer having opposing sides;

coupling a semiconductor chip to each of the opposing sides of the silicon interposer;

coupling the semiconductor chips on each side of the silicon interposer to one another through the silicon interposer by a number of micro-machined vias, wherein the micro-machined vias provide electrical connections between the opposing sides of the silicon interposer;

coupling a metal-to-semiconductor junction to at least one of the semiconductor chips, wherein the semiconductor includes an n-doped superlattice comprising alternating layers of $(PbTeSe)_m$ and $(BiSb)_n$ where m and n are the number of PbTeSe and BiSb monolayers per superlattice period.

66. A method for packaging an integrated circuit, comprising:

providing a silicon interposer having opposing sides;

coupling a semiconductor chip to each of the opposing sides of the silicon interposer;

coupling the semiconductor chips on each side of the silicon interposer to one another through the silicon interposer by a number of micro-machined vias, wherein the micro-machined vias provide electrical connections between the opposing sides of the silicon interposer;

coupling a metal-to-semiconductor junction to at least one of the of the semiconductor chips, wherein the semiconductor includes either an n or p-doped semiconductor alloy formed between Antimony (Sb) and a transition metal (T) from Group VIII, including Cobalt, Rhodium, and Iridium (Co, Rh, and Ir), and wherein the alloy has the general formula TSb_3.

67. A method for cooling an integrated circuit, comprising:

providing a silicon interposer having opposing sides;

coupling a first semiconductor chip to a first side of the silicon interposer;

coupling a second semiconductor chip to a second side of the silicon interposer, wherein a number of electrical connections through the silicon interposer couple the first semiconductor chip to the second semiconductor;

forming a metal-to-semiconductor junction which couples to the first semiconductor chip on the first side of the silicon interposer; and

passing current through the metal-to-semiconductor junction in a direction such that a Peltier cooling effect occurs adjacent to the first semiconductor chip.

68. The method of claim 67, wherein coupling a first semiconductor chip to the first side of the silicon interposer includes coupling a microprocessor chip to the first side.

69. The method of claim 67, wherein coupling a second semiconductor chip to the second side of the silicon interposer includes coupling a memory chip to the second side of the silicon interposer.

70. The method of claim 67, wherein forming a metal-to-semiconductor junction includes forming a Copper (Cu) and doped Bismuth Telluride (Bi_2Te_3) junction.

71. The method of claim 70, wherein forming a forming a Copper (Cu) and doped Bismuth Telluride (Bi_2Te_3) junction includes using vacuum evaporation to form a thin film of p-doped Bismuth Telluride (Bi_2Te_3).

72. The method of claim 67, wherein forming a metal-to-semiconductor junction includes forming a Copper (Cu) and doped Antimony Telluride (Sb_2Te_3) junction, wherein forming a forming a Copper (Cu) and doped Antimony Telluride (Sb_2Te_3) junction includes using vacuum evaporation to form a thin film of doped Antimony Telluride (Sb_2Te_3).

73. The method of claim 67, wherein forming a metal-to-semiconductor junction includes forming a Copper (Cu) and doped semiconductor junction, wherein the semiconductor is selected from Bismuth Telluride (Bi_2Te_3), Lead Telluride (PbTe), and Silicon Germanium (SiGe).

74. The method of claim 67, wherein forming a metal-to-semiconductor junction includes forming a metal-to-semiconductor junction which includes a doped superlattice junction, wherein the doped superlattice includes alternating layers of $(PbTeSe)_m$ and $(BiSb)_n$ where m and n are the number of PbTeSe and BiSb monolayers per superlattice period.

75. The method of claim 67, wherein forming a metal-to-semiconductor junction includes forming a metal-to-semiconductor junction wherein the semiconductor includes a complex oxide semiconductor, and wherein the complex oxide semiconductor includes Strontium (Sr) and Titanium (Ti).

76. A method for heating an integrated circuit, comprising:

providing a silicon interposer having opposing sides;

coupling a first semiconductor chip to a first side of the silicon interposer;

coupling a second semiconductor chip to a second side of the silicon interposer, wherein a number of electrical connections through the silicon interposer couple the first semiconductor chip to the second semiconductor;

forming a metal-to-semiconductor junction which couples to the first semiconductor chip on the first side of the silicon interposer; and

passing current through the metal-to-semiconductor junction in a direction such that a Peltier heating effect occurs adjacent to the first semiconductor chip.

77. The method of claim 76, wherein coupling a first semiconductor chip to the first side of the silicon interposer includes coupling a microprocessor chip to the first side.

78. The method of claim 76, wherein coupling a second semiconductor chip to the second side of the silicon interposer includes coupling a memory chip to the second side of the silicon interposer.

79. The method of claim 76, wherein forming a metal-to-semiconductor junction includes forming a metal-to doped semiconductor junction wherein the semiconductor is selected from Bismuth Telluride (Bi_2Te_3), Lead Telluride (PbTe), and Silicon Germanium (SiGe).

80. The method of claim 76, wherein forming a metal-to-semiconductor junction includes forming a metal and doped superlattice junction, wherein the doped superlattice includes alternating layers of $(PbTeSe)_m$ and $(BiSb)_n$ where m and n are the number of PbTeSe and BiSb monolayers per superlattice period.

81. The method of claim 76, wherein forming a metal-to-semiconductor junction includes forming a metal and doped complex oxide semiconductor, wherein the complex oxide semiconductor includes Strontium (Sr) and Titanium (Ti).

82. A method for cooling an integrated circuit, comprising:

providing a silicon interposer having opposing sides;

coupling a first semiconductor chip to a first side of the silicon interposer;

coupling a second semiconductor chip to a second side of the silicon interposer, wherein a number of electrical connections through the silicon interposer couple the first semiconductor chip to the second semiconductor;

forming a metal-to-semiconductor junction which couples to the first semiconductor chip on the first side of the silicon interposer, wherein forming the metal-to-semiconductor junction includes forming a Copper (Cu) and n or p-doped semiconductor junction wherein the semiconductor is selected from Bismuth Telluride (Bi_2Te_3), Lead Telluride (PbTe), and Silicon Germanium (SiGe); and

passing current through the metal-to-semiconductor junction in a direction such that a Peltier cooling effect occurs adjacent to the first semiconductor chip.